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The base-band binary data transmission system and BER estimation system based on neural network have been built. Few realizations of the neural network have been tested. While the discrete model and simulated version are working properly, some design/manufacture problems have occurred with the VLSI chip. If another version of the chip is going to be integrated, it would probably be modular (more than one chip) in order to have access to all relevant points for performance evaluation. Tests performed on a discrete NN system showed a lower accuracy than the simulations. The reason for this is the lower precision and stability of statistical moments calculated by analog circuitry. However, an analog system for BER measurement has been made operational, while its integration remains for future.

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IN-SERVICE BIT-ERROR-RATE MEASUREMENT IN COMMUNICATION NETWORKS

AFOSR Grant F49620-96-1-0306

Final Report

December 1999

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I. OBJECTIVE

The goal of this project is to build an on-line bit-error-rate (BER) measurement system based on a neural network. The system is initially trained for the expected range of channel disturbances and operates on-line (without interrupting data transmission). The interfacing part on the receiver side provides enough information for the neural network (NN) to recognize disturbances and estimate the BER.

II. ACCOMLISHMENTS

During the research, the following steps are performed:

1. Theoretical Analysis

Published as a conference paper: Elias Kosmatopoulos, Djuro Zrilic, "A Neural Network Model for Estimating Bit-Error-Rate in Digital Communication Systems", International Conference on Telecommunications ICT'98, Vol. III, Porto Carras, Greece, 21-25 June 1998, pp.296-300.
A modified version of this paper has been submitted for possible publication in IEEE Trans. on Vehicular Technology.
M. Narandzic, D. G. Zrilic: "Perceptron as a BER estimator", paper in preparation.

2. Simulation

Performances of the neural BER estimator are simulated in the presence of additive white gaussian noise (AWGN) and both fading and co-channel interference, all simultaneously. The results are shown in Figure 1 for different and randomly chosen disturbance combinations.

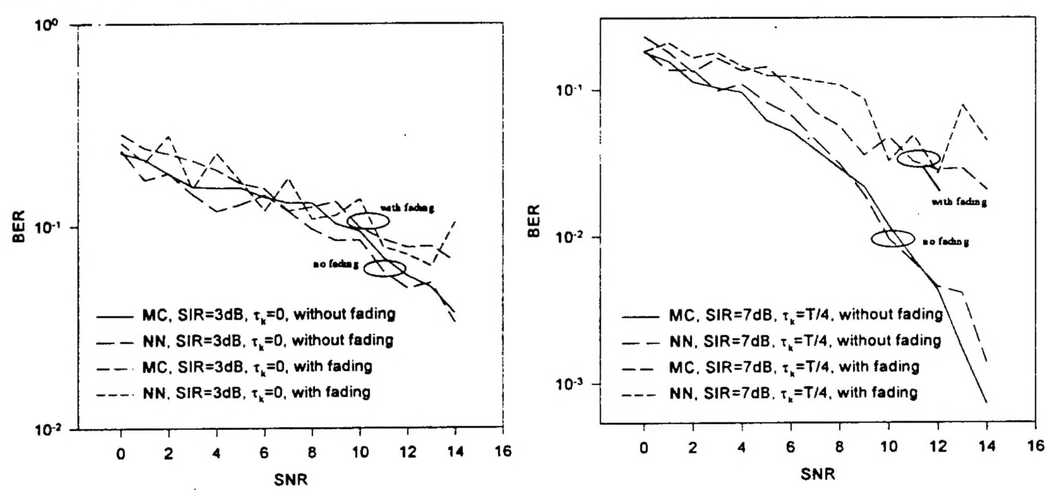


Figure 1 *NN BER Estimation (MC-Monte Carlo Method, NN-Neural Network Method, SIR-Signal-to-Interference Ration).*

3. Implementation

A block diagram of the overall system configuration under consideration is shown in Figure 1.

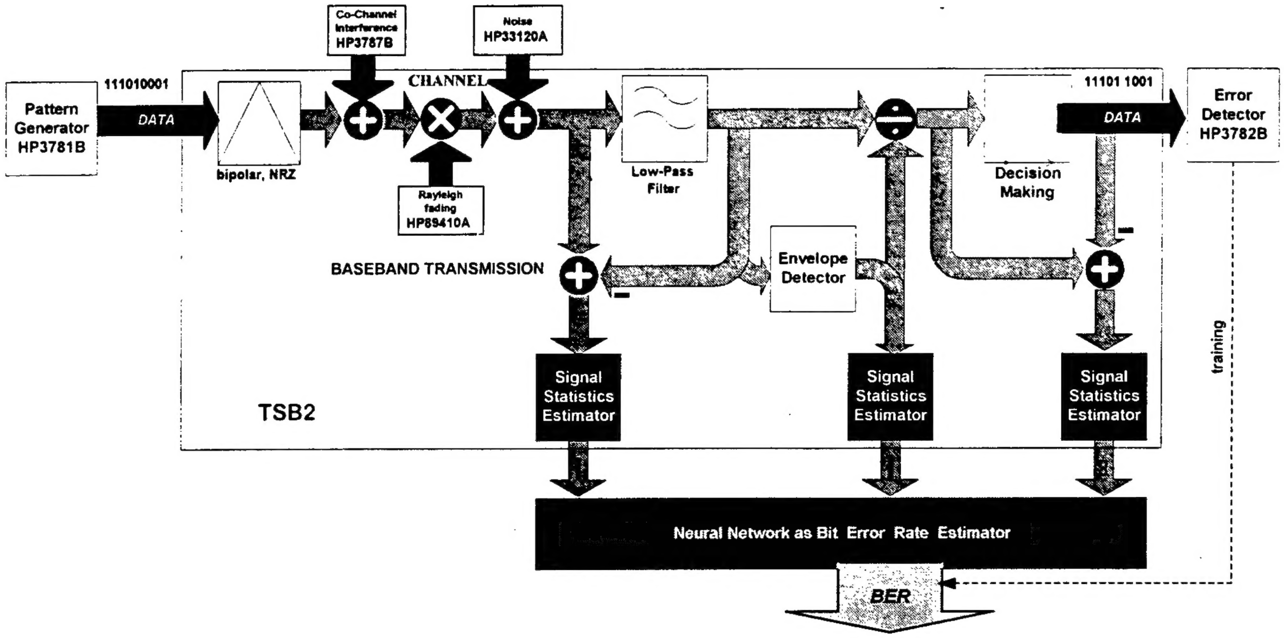


Figure 2 *Experimental setup.*

To verify the correctness of a signal-statistics estimator (SSE) approach, an ideal NN of the perceptron type (2-7-1) is simulated on the computer first. To interface SSE circuit, an 8-bit. converter is used. The input signal range for this converter was from 0 to 2.55V.

For different combinations of channel disturbances, statistical moments at the output of the SSE block are measured, while a known sequence is transmitted. At the same time, BER is measured on HP3782B Error Detector. These results are used to train a neural network programmed on the computer. A MATLAB environment is employed to train the NN using a back propagation algorithm. Interfacing is controlled by *cmex* (MATLAB executable written in C).

3.1 Implementation with NN emulated on personal computer (PC)

First, we have built a transmission system board TSB1 to evaluate binary base-band (BB) system performance in the presence of additive white Gaussian noise (Figure 3). Figure 4 shows the BER curve as a function of the noice variance. A circle represents a value of training pair, and a full line presents values that the NN learned. The network is trained using a back-propagation algorithm with an adaptive learning rate and momentum, until the sum-squared-error is less than 10^{-3}.

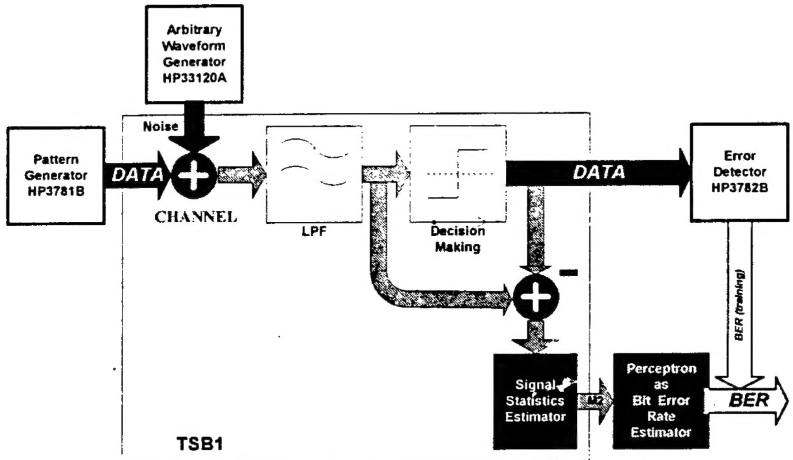


Figure 3 *Transmission System Board 1.*

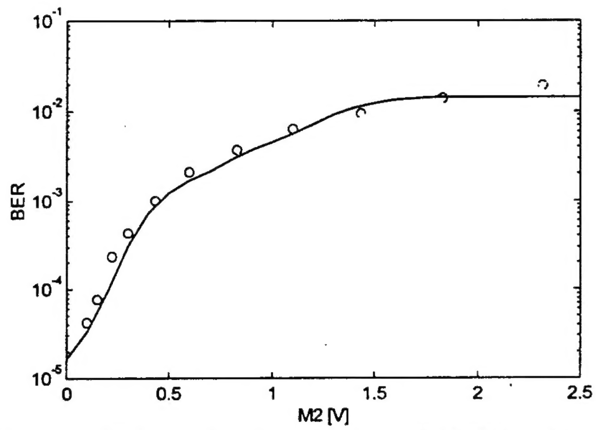
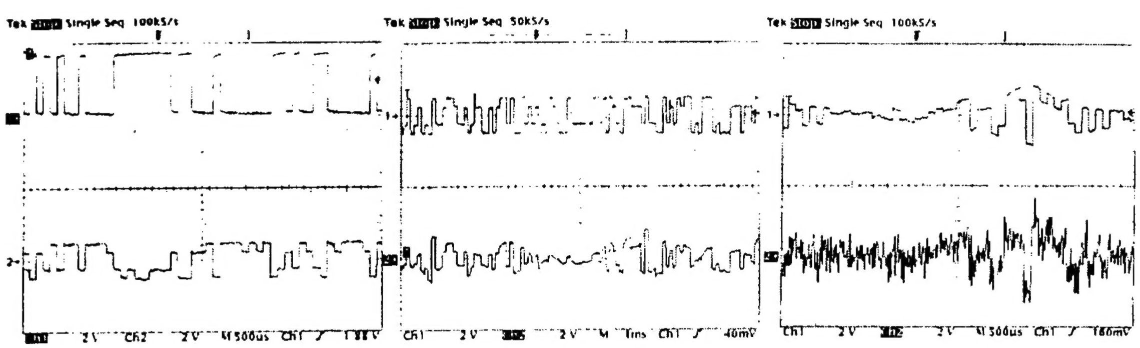


Figure 4 *BER as a function of estimated AWGN variance M2.*

Unit TSB2 (Figure 2) emulates AWGN, fading and co-channel interference. These disturbances are introduced into the communication channel by the following generators: HP3787B Digital Data Test, HP89410A Vector Signal Analyzer and HP33120A Arbitrary Waveform Generator. Figure 5 shows the waveforms corrupted by the following channel disturbances: (a) CCI, (b) Rayleigh fading and (c) AWGN.



(a) (b) (c)

Figure 5 *Radio channel emulation.*

A necessary training set for the NN was provided through the real measurement that was performed on the binary BB transmission system. To do so, we have performed the following necessary steps:

- The receiver communicates with the NN (stored in a PC) through a ADC, which accepts signal levels from 0 to 2.55V. Thus, the output range of SSE units have to be adjusted.
- Different combinations of disturbances are generated according to Figure 2. Statistical moments are measured at SSE unit outputs. For every recorded value of the moments, the BER is measured and recorded on the H3782B Error Detector. The pairs, consisting of statistical moments and the value of the BER, are representative examples for the neural network training set.
- Ideal NN is trained using the back propagation method. A block diagram of the NN is shown in Figure 6, and the result of a simulation (with real channel disturbances) is shown in Figure 7.

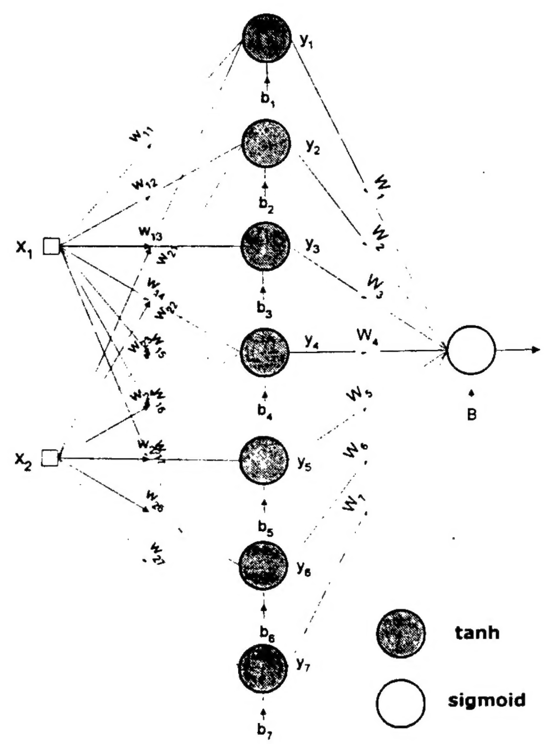


Figure 6 *Perceptron 2-7-1.*

The perceptron from Figure 6 is trained to estimate BER in the presence of AWGN and CCI, with their statistical variances as inputs. The training set contains examples for different combinations SIR={2, 3, 4, 5} dB and noise power P_N={0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10} dBm. After training is completed the sum-squared error settle to a value of 0.0251.

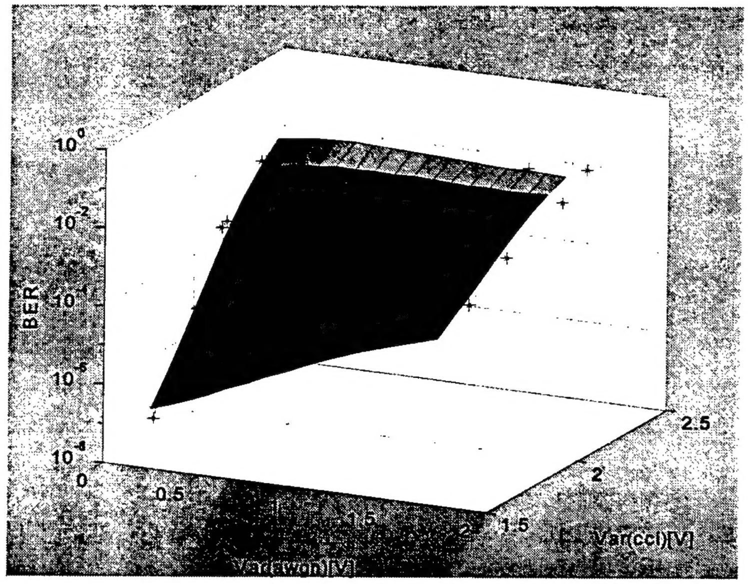


Figure 7 *Mapping learned by ideal 2-7-1 perceptron simulated on compluter.*

After NN training, the perceptron mapping is validated with new examples. In this case, it is a validation of the overall system, including Monte Carlo BER measurements, used resolution of disturbances for the training set, and the generalizing properties of the neural network.

3.2 Implementation when NN is realized in discrete form

While waiting for VLSI chip fabrication, a discrete model of the NN from Figure 6 was implemented. This unit was named DNN+MLT (discrete neural network with multipliers). Active components used for this purpose are four quadrant multipliers AD633J, operational transconductance amplifiers (OTA) CA3280E, and operational amplifiers LM741C. Realization of the hidden neuron with two inputs is shown in Figure 9.

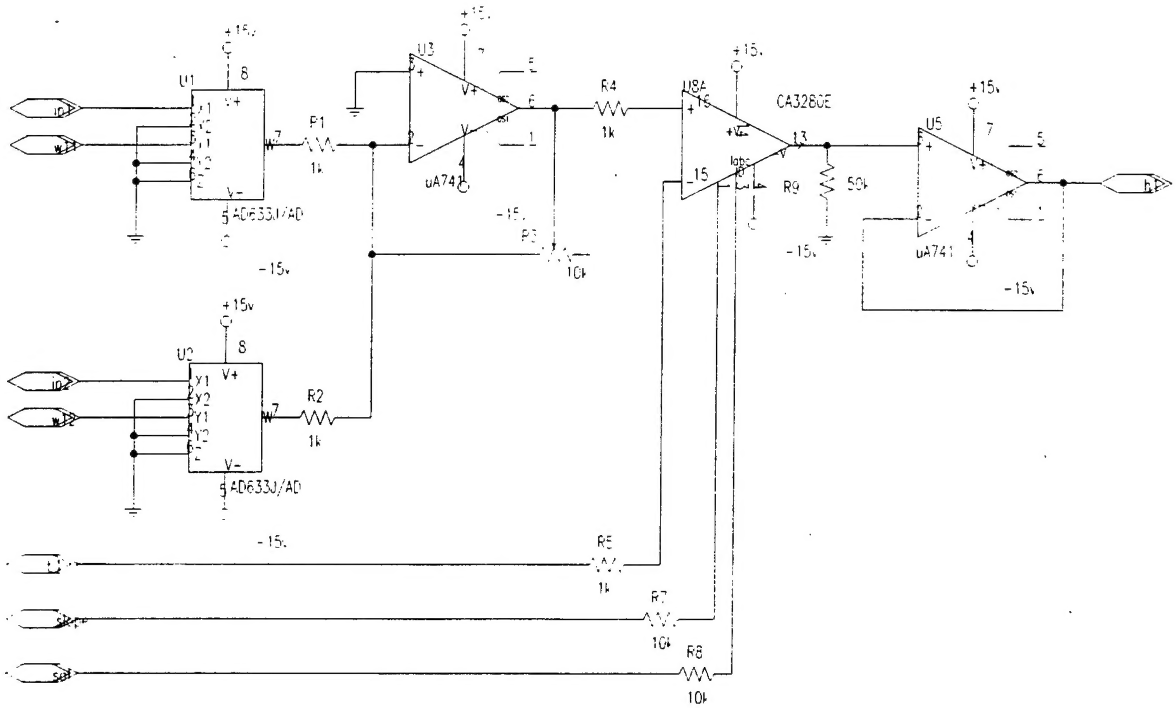


Figure 8 *Hidden neuron with two input synapses (w11 and w12), bias (b1) and adjustable slope and saturation level.*

The output neuron has a similar look; the only difference being that the hidden neuron has 2 inputs and 1 output, while the output neuron has 7 inputs and 1 output (Figure 6). The discrete model consists of two interconnected boards, DNN and MLT, while the supply is provided from the TSB2 board. The NN parameters, weights and biases, are generated externally by an array of potentiometers.

Discrete realization deals with analog neural network hardware which does not support training. Instead, hardware characteristics (such as multiplier constants, adder amplification and OTA transfer characteristics) are measured and included into the error back-propagation procedure simulated on the computer. Obtained weights and biases are then applied to the hardware model as external voltages. Because the transfer characteristic of the neuron in Figure 6 has a form of the hyperbolic tangent, we would like to approximate the OTA transfer function with

$$y(x) = \frac{a}{c + e^{-sx}} - b .$$

For each OTA, the transfer characteristic is measured and described by parameters *a*, *b*, *c*, and *s*. Figure 9 top curves represents transfer functions of the hidden layer neurons, and the bottom curve in Figure 9 presents the transfer function of the output neuron.

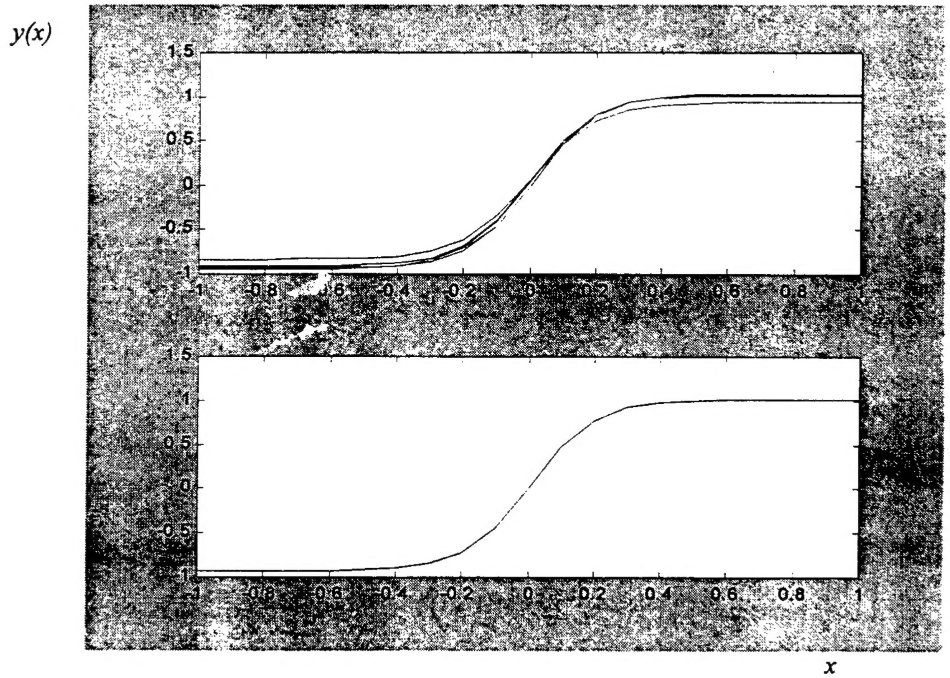


Figure 9 *Simulated OTA transfer characteristics of hidden and output network layer.*

For the optimized discrete model, back-propagation training can reach the sum-squared error equal to 0.0343. Figure 10 shows non-linear mapping which is learned by the simulated discrete neural network model. This result tells us that the discrete model is expected to show a performance that is very close to a real network simulated on the computer.

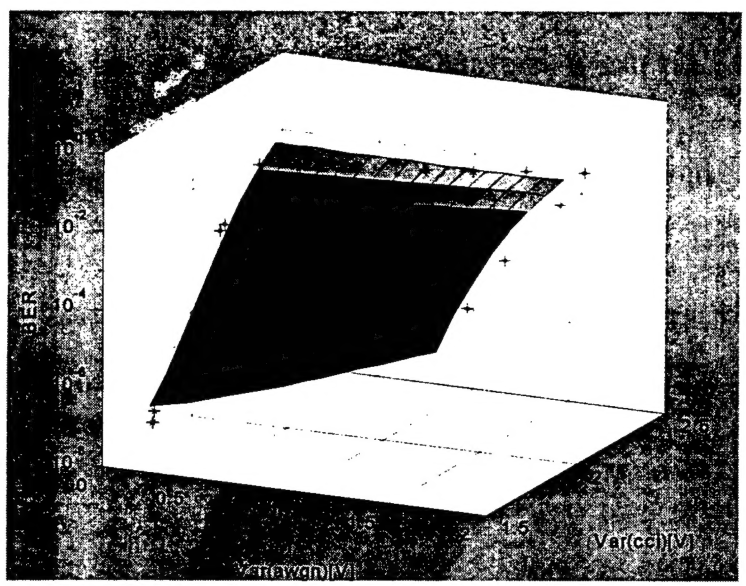


Figure 10 *Mapping of simulated perceptron discrete model with increased sensitivity.*

The values of weights and weights implemented in the discrete model are shown below.

$$
w = \begin{bmatrix} 1.6870 & 0.7643 \\ 0.6183 & -2.2609 \\ -0.0302 & -1.8507 \\ 1.7209 & -0.6855 \\ 1.8748 & 0.3662 \\ 1.3857 & 2.4768 \\ 1.5853 & -0.9715 \end{bmatrix},
$$

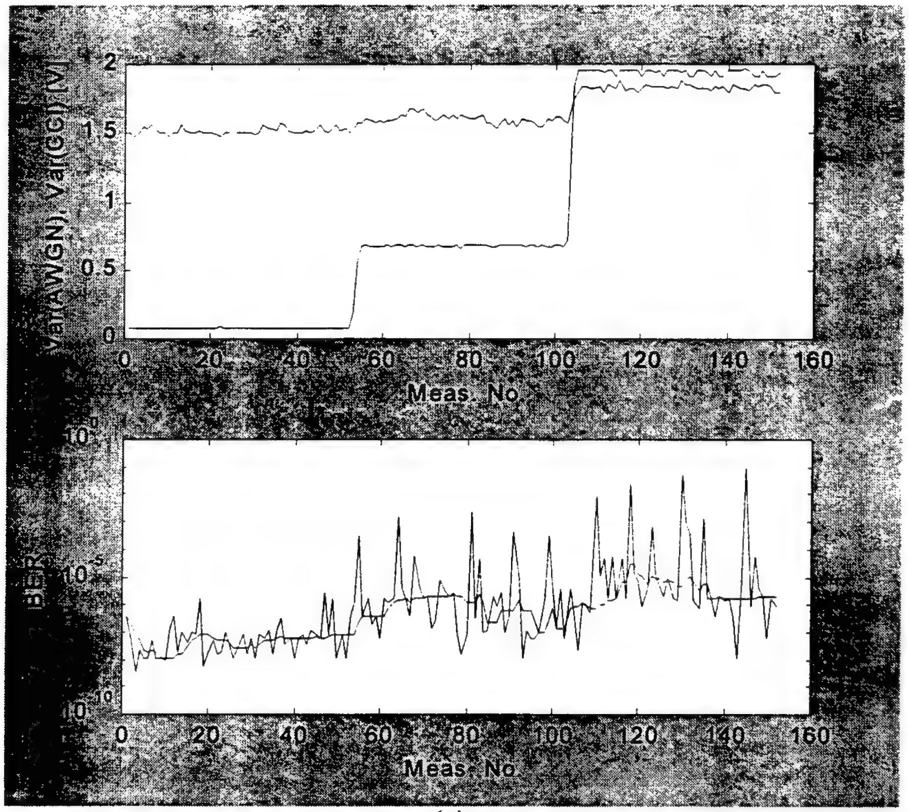
$$
W = \begin{bmatrix} 0.3666 & 0.6690 & 0.1077 & 0.2510 & 0.5175 & -0.8766 & 0.6525 \end{bmatrix},
$$

$$
b = \begin{bmatrix} 1.2538 \\ 0.4194 \\ -0.4793 \\ 0.7512 \\ 0.3079 \\ -0.4675 \\ 0.7192 \end{bmatrix},
$$

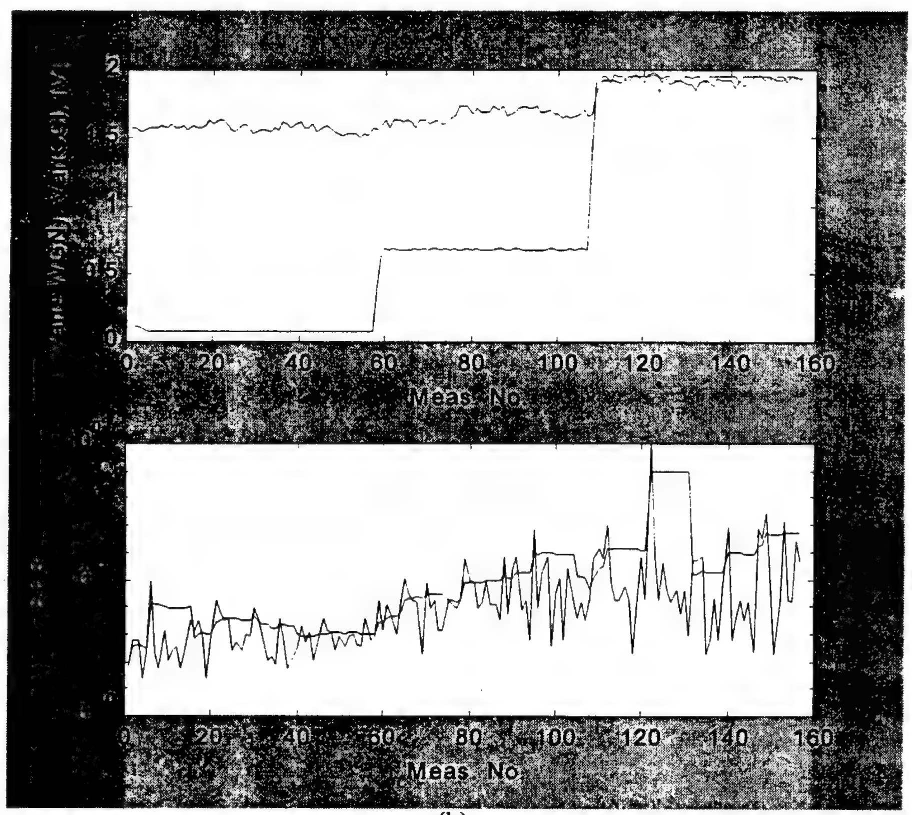
$$
B = -0.0531.
$$

These values are simulated and optimized on computer using a back-propagation algorithm:
w - the input weights of the hidden layer,
W - the weights of the output neuron,
b - the hidden neuron biases, and
B - the bias of the output neuron.

After adjusting these values on the discrete model, real performance of the BER estimator is monitored. The output of the NN is fed into an 8-bit ADC and then into the PC. Figure 11 shows the case when AWGN and co-channel interference are present as disturbances. Figure 11 (a) top shows values of the variances at the output of SSE units. It is possible to see three distinct regions; level of noise is first 0dBm, then increased to 5dBm and finally 10dBm. Figure 11 (a) bottom shows the value of the BER. We see from the median curve that the value of the BER is nearly 10^{-7}. After the increase of the noise variance, the BER value increased as well. A similar situation is shown in Figure 11 (b) as well; the only difference is that instead of a median operation a mean operation is performed on the row BER data.



(a)



(b)

Figure 11 *Results of the BER measurements on the discrete experimental model.*

3.3 VLSI neural network chip

We have fabricated the NN proposed in Figure 7. The layout and pin labels of the manufactured NN chip are shown in Figures 12 and 13 respectively.

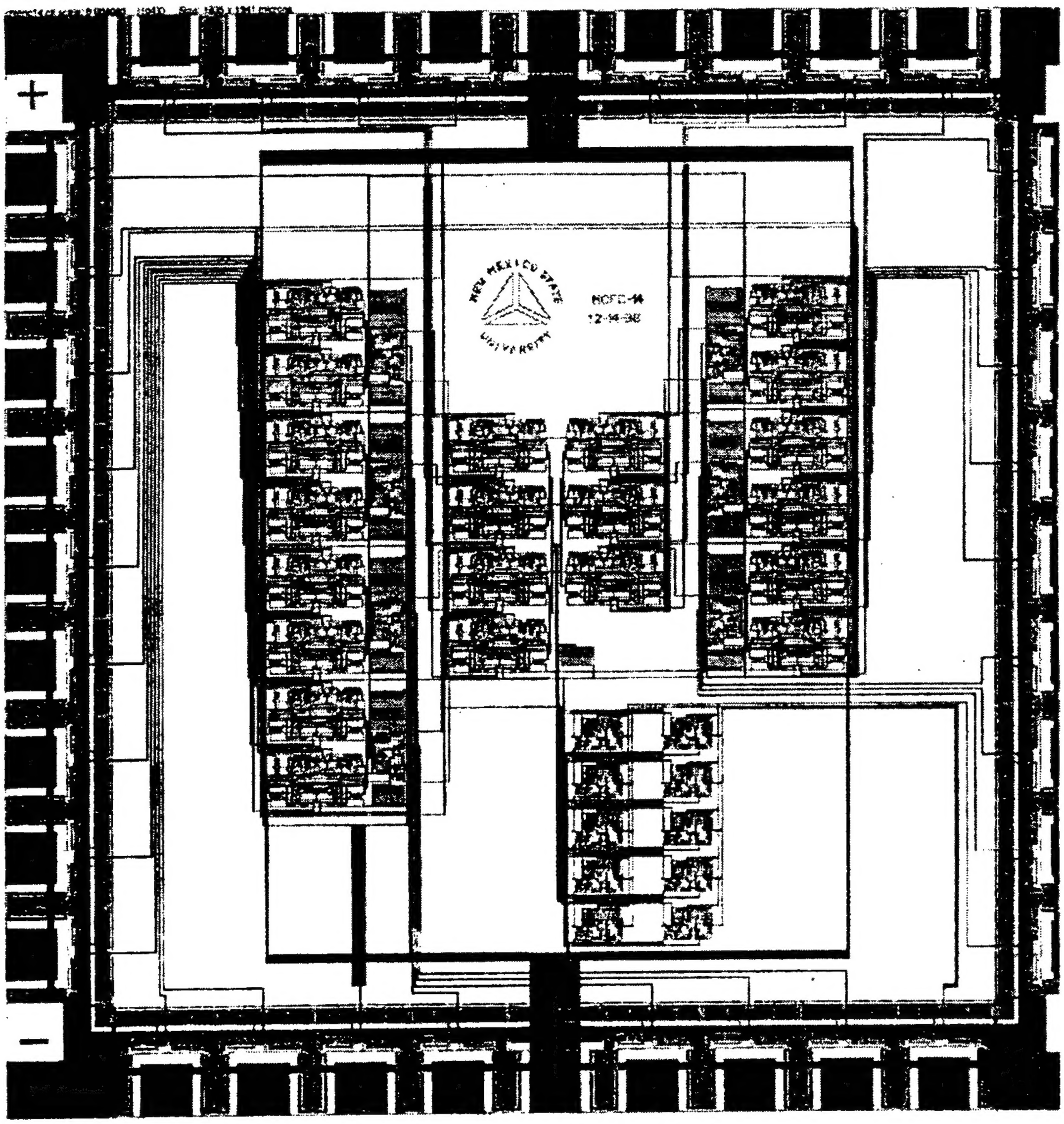


Figure 12 *Layout of the neural network chip.*

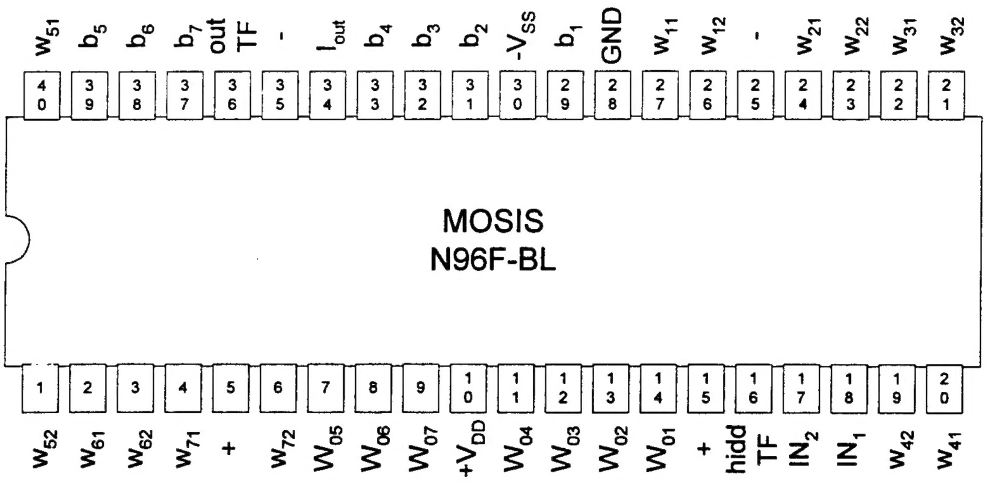


Figure 13 *Pins of manufactured neural network chip.*

Chip N96F-BL contains a fully connected two-layer perceptron with 2 inputs, 7 hidden neurons and one output (2-7-1). The main limitation of the size of the network that can fit into the chip comes from externally-supplied parameters. Commercially available custom chips support up to 40 pins. Due to lack of addressable and adjustable analog-voltage memories that could be implemented inside the chip, we have to provide all weights and biases externally. Summary of pins for N96F-BL are:

Number of pins	*Used for*
3	positive supply, V_{DD}
3	negative supply, V_{SS}
1	signal ground, GND
2	inputs: IN_1, IN_2
7x2=14	input weights of hidden neuron : w_{ji}, j=1..7, i=1,2
7	hidden neuron biases: b_j, j=1..7
1	adjustment of hidden neuron transfer function, hidd TF
7	output neuron weights: W_{0i}, i=1..7
1	adjustment of output neuron transfer function, out TF
1	output

TOTAL 40

Neural network chip evaluation are performed using a Karl Suss Analytical Prober PM5 and Mitutoyo Microscope Unit FS60. For that purpose, the NNC board containing the microchip socket, static electricity protection and interfacing ports, was constructed. Observed problems, that make chip unusable, are listed below:

- Chip performance is not optimized for the designed voltage supplies +2.75, –2.25. Figures 14 and 15 show an attempt to obtain a wider range of linearity of multipliers by changing the voltage supply. It is not possible to compensate offset and have good linearity.

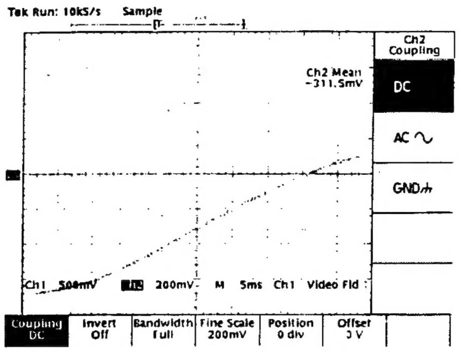


Figure 14 *$hi_1=f(X_{in2})$ for supply +5, - 2.8 chosen to reduce multiplier non-linearity.*

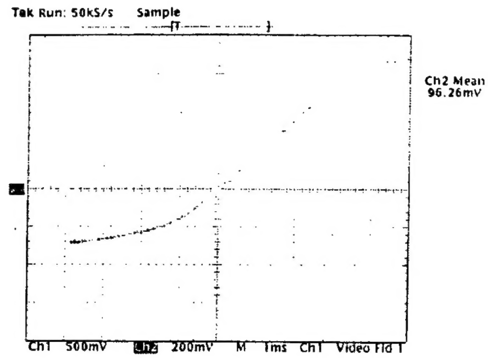


Figure 15 *$hi_1=f(X_{in2})$ for supply +5.08, 1.19 that reduce multiplier offset.*

- Hidden neuron #6 does not function at all.

- Hidden neuron biases b_i, i=1..7 are influencing voltage on all hidden neuron inputs. This causes a change in the slope and the offset of the multiplier transfer characteristics.

- Performance of the output neuron and multipliers representing its weights can not be evaluated due to lack of a measurement point. This point should provide access to the input of the output neuron and though it is present on the layout it does not exist on the chip.

This is the third attempt to fabricate a NN VLSI chip. In our opinion, special care must be dedicated to the proper VLSI layout and to the process of fabrication at the MOSIS foundry.

III. PERSONNEL SUPPORTED

Dr. Djuro George Zrilic, NMHU,

Dr. Jaime Ramirez, NMSU,

Milan Narandzic, MS, NMHU,

STUDENTS SUPPORTED

Jeromy Payton,

Joseph Winkles,

Lawren Kayssing.

IV. TRANSITIONS

None

V. OPEN PROBLEMS

Three attempts for costume chip integration of the NN have been made. The new version has been recently tested and measurements showed that further improvements are necessary to make the chip operational.

VI. CONCLUSION

The base-band binary data transmission system and BER estimation system based on neural network have been built. Few realizations of the neural network have been tested. While the discrete model and simulated version are working properly, some design/manufacture problems have occurred with the VLSI chip. If another version of the chip is going to be integrated, it would probably be modular (more than one chip) in order to have access to all relevant points for performance evaluation. Tests performed on a discrete NN system showed a lower accuracy than the simulations. The reason for this is the lower precision and stability of statistical moments calculated by analog circuitry. However, an analog system for BER measurement has been made operational, while its integration remains for future.

VII. ACKNOWLEDGMENT

NMHU and PI wish to express sincere gratitude to the AIR FORCE Research Office and its people for support and trusting our minority institution. The financial support given to us over the last three years has enabled us to gain new knowledge and experience, to form a new communication laboratory (equipped with a new instruments), and to involve a number of our undergraduates in research. We are particularly thankful for the help and leadership of Dr. Jon Sjogren.